Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (previously presented): A method of employing a Rake receiver in a wireless radio access system to a radio uplink link which results in a significant increase in data transference in a spread modulation signal, the method comprising:

(a) receiving a spread modulation signal and presenting it to a plurality of Rake fingers, wherein each Rake finger processes the spread modulation signal, each Rake finger delaying the spread modulation signal by a differing amount of time;

(b) multiplying the delayed spread modulation signal with a first reference signal producing a control bit signal;

(c) multiplying the delayed spread modulation signal with a second reference signal producing a data signal;

(d) delaying said data signal producing a delayed data signal;

(e) multiplying said delayed data signal with weights produced by a frequency offset estimator and a complex weight gain generator to produce a first set of data; and

(f) summing the outputs of all of the Rake fingers, producing data symbols and control bit symbols.

2. (previously presented): The method of claim 1 wherein the frequency offset estimator performs a frequency offset estimation determined by averaging blocks of pilot signals.

3. (previously presented): The method of claim 2 wherein said frequency offset estimation is determined using a sliding window averaging algorithm.

4. (previously presented): The method of claim 2 wherein said frequency offset estimation is determined using a recursive filter.

5. (previously presented): A Rake receiver used in a wireless communications system, the Rake receiver comprising:

(a) means for receiving a spread modulation signal and presenting it to a plurality of Rake fingers, wherein each Rake finger processes the spread modulation signal, each Rake finger delaying the spread modulation signal by a differing amount of time;

(b) means for multiplying the delayed spread modulation signal with a first reference signal producing a control bit signal;

(c) means for multiplying the delayed spread modulation signal with a second reference signal producing a data signal;

(d) means for delaying said data signal producing a delayed data signal;

(e) means for multiplying said delayed data signal with weights produced by a frequency offset estimator and a complex weight gain generator to produce a first set of data; and

(f) means for summing the outputs of all of the Rake fingers, producing data symbols and control bit symbols.

6. (previously presented): The receiver of claim 5 wherein the frequency offset estimator performs a frequency offset estimation determined by averaging blocks of pilot signals.

7. (currently amended): The receiver of ~~claim 5~~ claim 6 wherein said frequency offset estimation is determined using a sliding window averaging algorithm.

8. (currently amended): The receiver of ~~claim 5~~ claim 6 wherein said frequency offset estimation is determined using a recursive filter.

9. (previously presented): A wireless receiver/transmitter unit (WTRU) used in a wireless communications system, comprising:

(a) means for receiving a spread modulation signal and presenting it to a plurality of Rake fingers, wherein each Rake finger processes the spread modulation signal, each Rake finger delaying the spread modulation signal by a differing amount of time;

(b) means for multiplying the delayed spread modulation signal with a first reference signal producing a control bit signal;

(c) means for multiplying the delayed spread modulation signal with a second reference signal producing a data signal;

(d) means for delaying said data signal producing a delayed data signal;

(e) means for multiplying said delayed data signal with weights produced by a frequency offset estimator and a complex weight gain (CWG) generator to produce a first set of data; and

(f) means for summing the outputs of all of the Rake fingers, producing data symbols and control bit symbols.

10. (previously presented): The WTRU of claim 9 wherein the frequency offset estimator performs a frequency offset estimation determined by averaging blocks of pilot signals.

11. (previously presented): The WTRU of claim 10 wherein said frequency offset estimation is determined using a sliding window averaging algorithm.

12. (previously presented): The WTRU of claim 10 wherein said frequency offset estimation is determined using a recursive filter.

13. (previously presented): A Rake receiver used in a wireless communications system, the Rake receiver comprising:

(a) a first combiner;

(b) a second combiner; and

(c) a plurality of Rake fingers for receiving and processing a spread modulation signal, each Rake finger comprising:

(i) a first despreader having a first input for receiving the spread modulation signal, a second input for receiving a pilot signal and an output for outputting despread pilot symbols;

(ii) a second despreader having a first input for receiving the spread modulation signal, a second input for receiving a data signal and an output for outputting despread data symbols;

(iii) a data bit processor having an input for receiving the despread pilot symbols and an output for outputting processed pilot symbols to be combined in the first combiner with other similarly processed pilot symbols outputted by other ones of the Rake fingers;

(iv) a frequency offset estimator having an input for receiving the despread pilot symbols and an output for outputting a frequency offset estimation signal;

(v) a complex weight gain generator in communication with the output of the first despreader and the output of the frequency offset estimator, the complex weight gain generator having a first input for receiving the despread pilot

symbols, a second input for receiving the frequency offset estimation signal, and an output for outputting weighted symbols;

(vi) a delay element in communication with the output of the second despreader for delaying the despread data symbols, the delay element having an output for outputting the delayed despread data symbols; and

(vii) a multiplier in communication with the output of the delay element and the output of the complex weight gain generator, the multiplier having a first input for receiving the delayed despread data symbols and a second input for receiving the weighted symbols and outputting processed data symbols to be combined in the second combiner with other similarly processed data symbols outputted by other ones of the Rake fingers.

14. (previously presented): The Rake receiver of claim 13 wherein the pilot signal comprises a dedicated physical common channel (DPCCH).

15. (previously presented): The Rake receiver of claim 14 wherein the first despreader outputs despread DPCCH symbols.

16. (previously presented): The Rake receiver of claim 13 wherein the data signal comprises a dedicated physical data channel (DPDCH).

17. (previously presented): The Rake receiver of claim 16 wherein the second despreader outputs despread DPDCH symbols.

18. (previously presented): The Rake receiver of claim 14 wherein the data bit processor outputs transmit power control (TPC) and feedback information (FBI) used for closed loop transmission diversity.

19. (currently amended): An integrated circuit (IC) which processes spread modulation signals, the IC comprising:

~~(a) an input for receiving a spread modulation signal;~~

(a) ~~(b)~~ a first combiner;

(b) ~~(c)~~ a second combiner; and

(c) ~~(d)~~ a plurality of Rake fingers for receiving and processing a spread modulation signal, each Rake finger comprising:

(i) a first despreader having a first input for receiving the spread modulation signal, a second input for receiving a pilot signal and an output for outputting despread pilot symbols;

(ii) a second despreader having a first input for receiving the spread modulation signal, a second input for receiving a data signal and an output for outputting despread data symbols;

(iii) a data bit processor having an input for receiving the despread pilot symbols and an output for outputting processed pilot symbols to be combined in the first combiner with other similarly processed pilot symbols outputted by other ones of the Rake fingers;

(iv) a frequency offset estimator having an input for receiving the despread pilot symbols and an output for outputting a frequency offset estimation signal;

(v) a complex weight gain generator in communication with the output of the first despreader and the output of the frequency offset estimator, the complex weight gain generator having a first input for receiving the despread pilot symbols, a second input for receiving the frequency offset estimation signal, and an output for outputting weighted symbols;

(vi) a delay element in communication with the output of the second despreader for delaying the despread data symbols, the delay element having an output for outputting the delayed despread data symbols; and

(vii) a multiplier in communication with the output of the delay element and the output of the complex weight gain generator, the multiplier having a first input for receiving the delayed despread data symbols and a second input for receiving the weighted symbols and outputting processed data symbols to be combined in the second combiner with other similarly processed data symbols outputted by other ones of the Rake fingers.

20. (previously presented): The IC of claim 19 wherein the pilot signal comprises a dedicated physical common channel (DPCCH).

21. (previously presented): The IC of claim 20 wherein the first despreader outputs despread DPCCH symbols.

22. (previously presented): The IC of claim 19 wherein the data signal comprises a dedicated physical data channel (DPDCH).

23. (previously presented): The IC of claim 22 wherein the second despreader outputs despread DPDCH symbols.

24. (previously presented): The IC of claim 19 wherein the data bit processor outputs transmit power control (TPC) and feedback information (FBI) used for closed loop transmission diversity.